A 30-GHz Monolithic Receiver

LOUIS C. T. LIU, MEMBER, IEEE, CAROL S. LIU, MEMBER, IEEE, JOEL R. KESSLER, MEMBER, IEEE, SHING-KUO WANG, MEMBER, IEEE, AND CHING-DER CHANG, MEMBER, IEEE

Abstract—**Several monolithic integrated circuits have been developed to make a 30-GHz receiver. The receiver components include a low-noise amplifier, an IF amplifier, a mixer, and a phase shifter. The LNA has a 7-dB noise figure with over 17 dB of associated gain. The IF amplifier has a 13-dB gain with a 30-dB control range. The mixer has a conversion loss of 10.5 dB. The phase shifter has a 180° phase shift control and a minimum insertion loss of 1.6 dB.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMIC's) are becoming easier to manufacture and potentially less costly due to recent advances in GaAs material and processing [1], [2]. However, at frequencies above 30 GHz, monolithic technology is not yet mature, and only a few papers have been published [3]–[9]. Monolithic IC development at these frequencies is hampered by a number of key problems, including device performance, device measurement and modeling, monolithic component realization, and IC measurement.

In this paper, we describe the systematic development of a 30-GHz receiver using monolithic chips for a communication antenna feed array [10]. This includes the design, fabrication, and measurement results of each submodule chip and of the complete receiver module. This is the first *Ka*-band receiver module using all monolithic chips. This is the first step towards fabricating an entire module on a single GaAs chip.

II. Receiver Design

The object of this work was to develop a 27.5-to-30-GHz receiver module for use in a phased-array antenna. The modules need variable gain and phase so that the beam can be aimed in any direction. Fig. 1 shows the system block diagram of the receiver module. A two-stage, low-noise amplifier (LNA) sets the noise figure of the system, a mixer chip downconverts the signal to an IF band of 4 to 6.5 GHz, a 5-bit phase shifter is used at the LO frequency, and a variable-gain IF amplifier provides amplitude control. Shifting the phase of the entire RF band causes phase errors due to the frequency and amplitude variations over the band. These errors are minimized by designing the phase shifter in the LO signal path where only the path of the one LO frequency will be shifted. The design goals of this receiver were 5-dB noise figure, 10-dB gain, and six gain states.

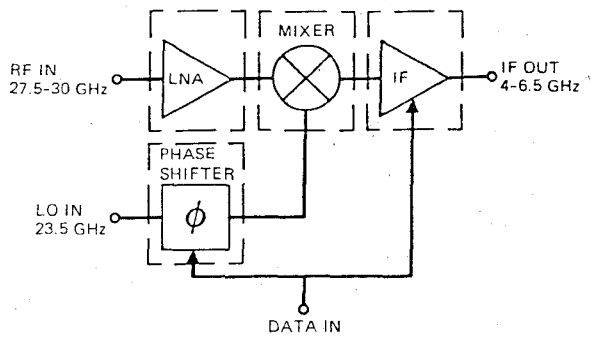

Fig. 1. Receiver module block diagram.

Fig. 2. Monolithic components for 30-GHz receiver module.

All four monolithic chips have been developed. Fig. 2 shows these chips and illustrates the potential for an extremely compact receiver module. The details of each chip and the receiver integration will be discussed in the following sections.

III. Low-Noise Amplifier Chip

The low-noise amplifier design has been presented before [3]. The amplifier chip shown in Fig. 3 uses two 0.25×150-μm FET's. They were fabricated using an active layer produced by silicon ion implantation at 100 keV into a LEC substrate. All layers were fabricated by optical lithography except for the gate definition. Electron beam lithography was employed to write the gate structure into a

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L. C. T. Liu was with the Microwave Products Division, Hughes Aircraft Company, Torrance CA. He is now with TRW.

C. S. Liu, J. R. Kessler, S. K. Wang, and C. D. Chang are with the Microwave Products Division, Hughes Aircraft Company, Torrance, CA 90509.

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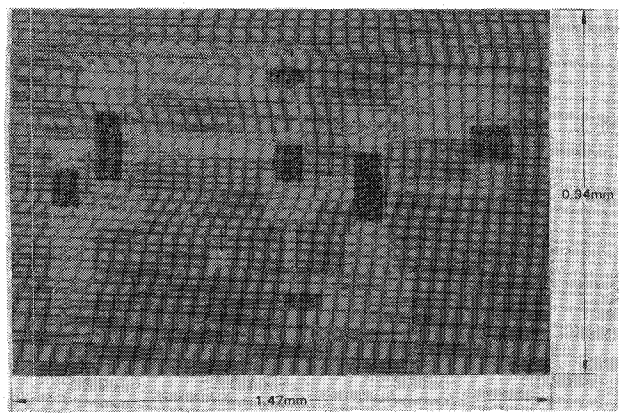

Fig. 3. Photo of *Ka*-band monolithic low-noise amplifier chip.

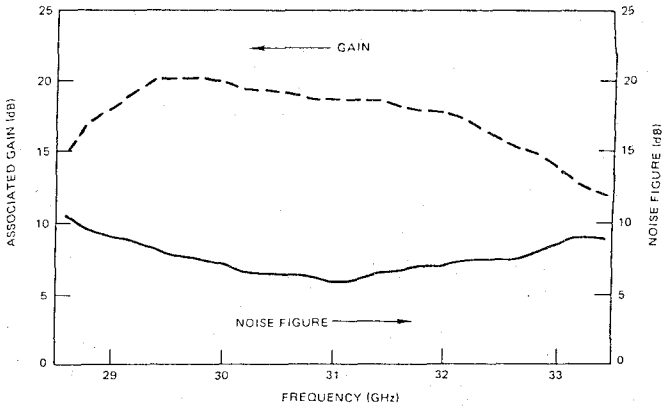

Fig. 5. Measured performance of *Ka*-band monolithic LNA.

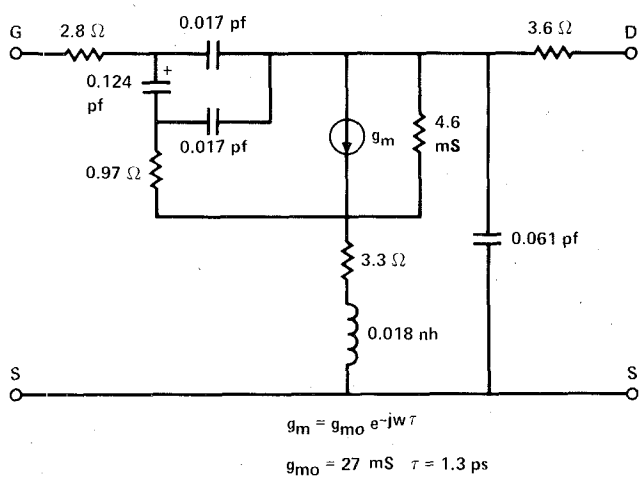

Fig. 4. 25-μm FET equivalent circuit model and element values for low-noise bias.

multilayer resist. This technique produces a very uniform and repeatable mushroom-shaped gate structure. The "footprint" of the gate can be varied from 0.1 μm to 0.3 μm consistently. One characteristic feature of this gate process is a gate height of about 0.5 μm, which yields a fairly large gate aspect ratio. The advantage of this type of gate is that a greatly enlarged cross-sectional area and a resulting reduction of gate resistance are obtained.

To design an amplifier, a representative device equivalent circuit model of the FET is required. This equivalent circuit model, shown in Fig. 4, is generated from measured device *S*-parameters by averaging the equivalent circuit element values of a number of different FET's. This set of average element values can then be considered as a typical equivalent circuit and can be used to design the amplifier.

The LNA input matching network consists of a shunt-shorted stub and a cascaded line to provide a noise figure match at the input of the device at 29 GHz. An optimization routine was used to obtain the optimum element values for the input matching network to provide a noise match from 27.5 to 30 GHz. During the optimization, the effects of the shunt MOM capacitor and the loss of the microstrip line were included.

By cascading the optimum input matching network and the first device, a new set of output port circuit parameters were obtained. An interstage matching network was synthesized to provide a gain match between the output port and the input of the second 1/4-μm device, which is biased at I_{dss}. The interstage matching network has three reactive transmission-line sections, which include two cascaded lines and a shunt-shorted stub. The shunt stub is split into two identical sections with a dc-blocking capacitor inserted between them. Two RF-bypassing capacitors are used for grounding the shunt stubs. Similarly, an output matching network consisting of a cascaded line and a shunt-shorted stub was synthesized to provide a gain match between the output port of the second device and the 50-Ω load. The complete amplifier circuit was then reoptimized to obtain a flat overall gain response across the frequency band of interest. The LNA chip has demonstrated an average noise figure of 7 dB with an associated gain of 17 dB. The gain response and the noise figure are illustrated in Fig. 5.

IV. IF Amplifier

A two-stage resistive feedback IF amplifier was developed to operate from 2 to 6.5 GHz. The schematic of the amplifier is shown in Fig. 6. Microstrip transmission lines were used for RF matching because of their low loss, low dispersion, and useful impedance range. The amplifiers used two 0.8×300-μm-gate FET's. The FET equivalent circuit model was calculated from the measured *S*-parameter data of discrete FET's.

MOM overlay capacitors were used for RF bypassing and dc blocking. Airbridges were used to interconnect the source pads and to connect the microstrip lines to the top plate of the overlay capacitors. A substrate thickness of 0.1 mm was chosen to facilitate the fabrication of via hole with high yield. The via hole ground allowed greater flexibility in the layout of the amplifier because grounds can be placed almost anywhere on a circuit rather than only at the substrate edges. The circuit was analyzed using computer simulation and FET equivalent circuit models. The completed amplifier chip is shown in Fig. 7, and the entire chip size is 1.1×1.9×0.1 mm.

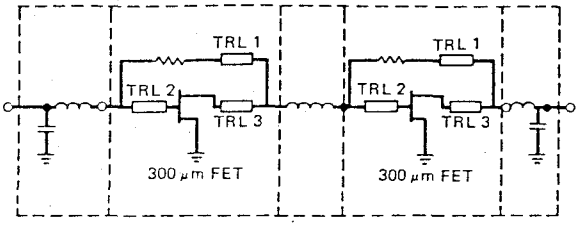

Fig. 6. Schematic of the IF amplifier.

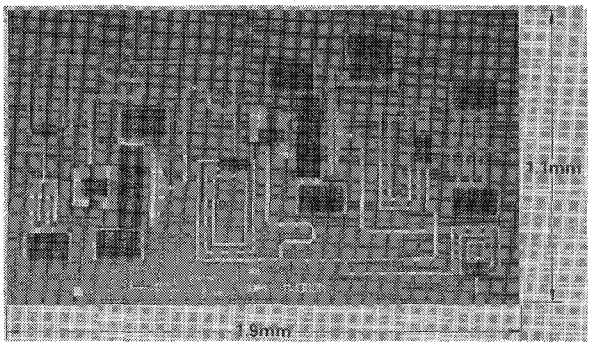

Fig. 7. Photograph of monolithic IF amplifier chip.

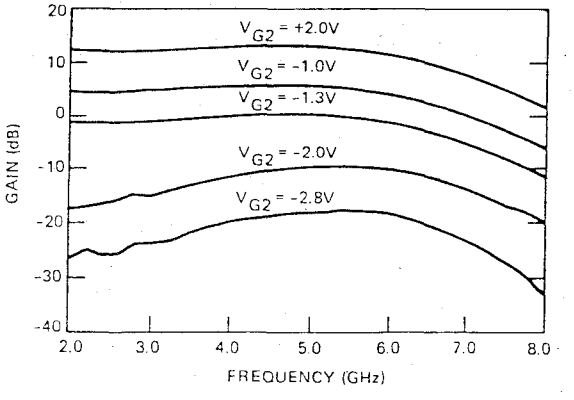

Fig. 8. Measured performance of variable-gain IF amplifier.

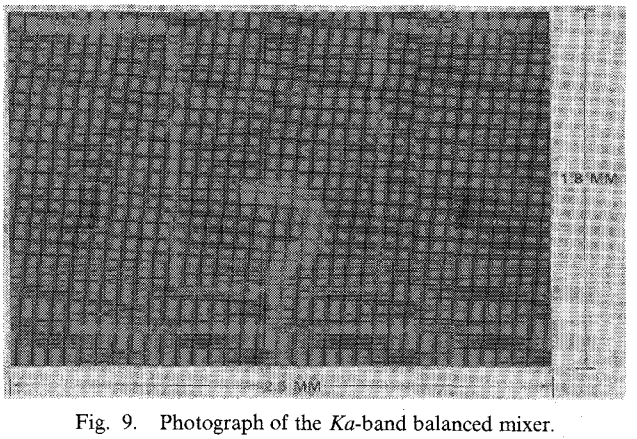

Fig. 9. Photograph of the *Ka*-band balanced mixer.

The passive components include thin-film resistors, MOM and interdigitated capacitors, spiral inductors, and via holes. The MOM capacitors and the resistors were fabricated with tantalum pentoxide and tantalum nitride films, respectively. The capacitance value per area of the MOM capacitor with a 2000-Å-thick tantalum pentoxide

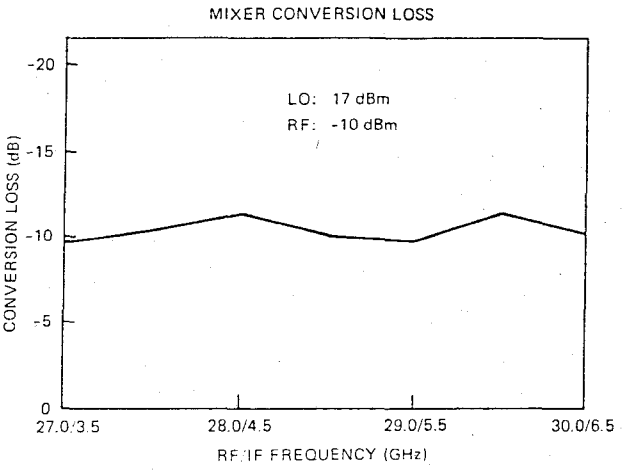

Fig. 10. Measured conversion loss of the *Ka*-band monolithic mixer.

layer is 1000 pF/mm^2, and the resistance of the TaN resistor is about 25 Ω per square.

The active devices are a standard MESFET and a dual-gate MESFET with 0.8×300-μm gate fingers fabricated by contact photolithography. Varying the bias of the second gate of the dual-gate MESFET controls the gain. Measured data show that this amplifier has a gain control range of over 30 dB with a maximum gain of 13 dB (Fig. 8). The noise figure was less than 5 dB across the band at all gain levels. Also, VSWR and phase variations were minimal at all gain control levels.

V. Mixer

The mixer is a balanced design which consists of a pair of Schottky barrier diodes and a large coupler. The photograph of a complete mixer submodule is shown in Fig. 9. The coupler isolates the signal and LO ports. A single-pole, low-pass filter with quarter-wavelength stubs is employed in the IF port to reject RF and LO signals. DC returns are accomplished through via holes. Since the goal is to integrate diodes FET's on the same GaAs chip for future single-chip receiver modules, a selective and multiple-charge ion implantation was used to fabricate the diodes. A N/N+ implant profile with a heavy selective N+ implant in the ohmic area was used. The resulting diodes had a cutoff frequency of up to 550 GHz and an ideality of 1.2.

The measured data indicate that the mixer has a conversion loss of about 10.5 dB across the frequency band (Fig. 10). The impedance mismatch at the input of the diodes necessitated high LO power to turn the diodes on. Tuning the output also lowers the conversion loss. The next iteration will therefore have an improved resistive input match, and the circuit will also allow the diodes to be dc-biased to further reduce the necessary LO power. The output circuit will accommodate tuning stubs for a better reactance match.

VI. Phase Shifter

The phase shifter consists of an interdigitated Lange coupler together with a pair of GaAs Schottky barrier

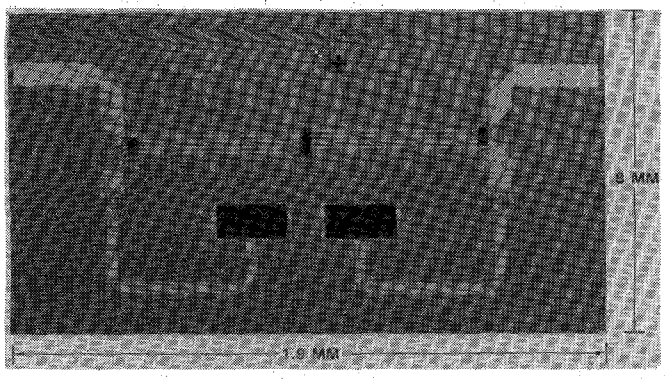

Fig. 11. Photograph of 23.5-GHz phase shifter.

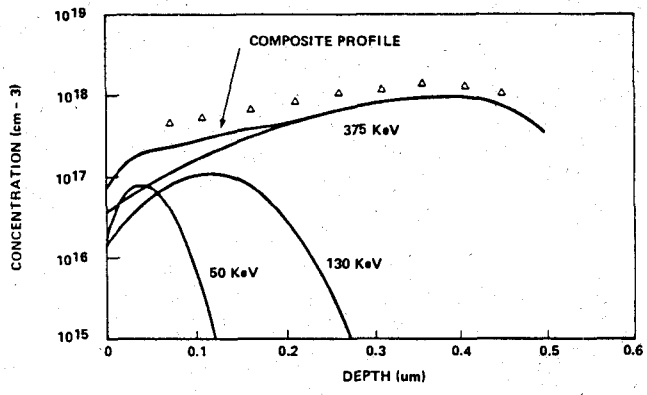

Fig. 12. Composite profile of N-on$N+$ prepared by ion implantation technique.

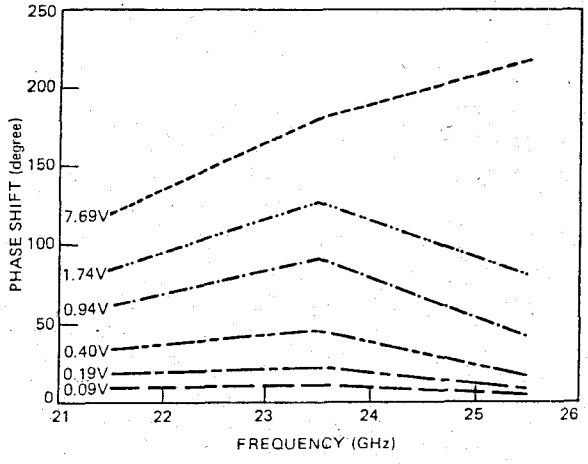

Fig. 13. Measured performance of the monolithic phase shifter.

diodes to form a small, high-yield transmission phase shifter, as shown in Fig. 11. The varactor diodes were fabricated on an active layer formed by multiple-charge ion implantation into an LEC substrate. The calculated and measured doping profile is shown in Fig. 12. Three different implantation energy levels are 50 keV, 130 keV, and 375 keV, respectively. The typical ideality factor is about 1.2; the series resistance of the diode is about 6 Ω, and the diode capacitance is in the range of 40 fF. The cutoff frequencies of these devices range up to 450 GHz. In addition, a 3 to 1 (60 fF to 20 fF) capacitance swing is obtained by varying the bias voltage. The phase shift at

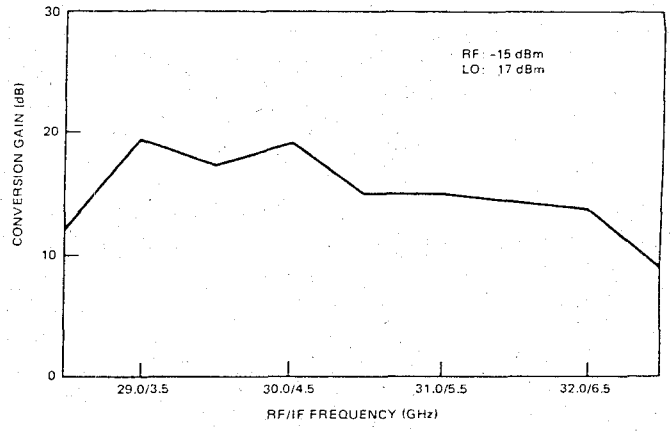

Fig. 14. Measured conversion gain of mixer, LNA, and IF amplifier.

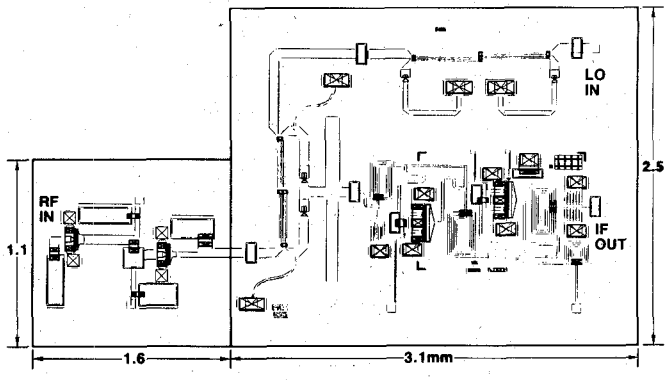

Fig. 15. Preliminary layout of integrated monolithic receiver chip and LNA.

23.5 GHz can be accomplished with the diode bias voltage varying from 0 to 8 V, as shown in Fig. 13. The insertion loss is 1.6 dB at the highest point of reverse bias (8 V).

VII. Receiver Integration

These four monolithic submodule chips can be connected with bond wires and can be mounted on a compact test carrier. We have fabricated a test carrier and a housing which will provide all the necessary blocking capacitors and bias lines to facilitate the receiver evaluation. To estimate the performance of this integration, three devices, each in their own housing, were connected together and tested. The measurement of these chips, the LNA, mixer, and IF amplifier, indicates a conversion gain of about 15 dB (Fig. 14).

Our goal is to integrate the IF amplifier, mixer, and phase shifter into one chip. The LNA will be a separate chip. This scheme will result in the highest yield with the best performance. Since the goal of submodule development is aiming at the proof-of-concept, the physical layout of each submodule was not optimized for wafer real estate. In the module integration, we will optimize the layout design to reduce the chip area and better utilize the wafer real estate. The preliminary CAD layout for the receiver is shown in Fig. 15. To integrate the submodules, we have to fabricate FET's and diodes on the same wafer. Multiple ion doses and energies will be selectively implanted into a

LEC substrate to form the active areas for the FET's and diodes. These active areas can be isolated with proton bombardment. Fabrication of the passive components is a standard MMIC process.

VIII. Conclusions

Four monolithic chips for a 30-GHz receiver module have been developed for communication-antenna feed arrays. A selective and multiple-charge ion implantation technique has been developed which permits the integration of both diodes and FET's on the same chip. This technique holds the promise of making a fully monolithic receiver module. This single-chip approach has potential for inexpensive fabrication of receiver modules. This in turn shall promote the use of future satellite communication systems which require large quantities of identical receiver modules.

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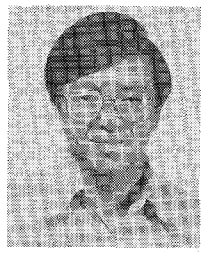

Louis C. T. Liu (S'77–M'81) received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 1974, and M.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1978 and 1981, respectively.

While at Cornell, he worked as a graduate research assistant in the field of microwave broad-band circuit synthesis and design with applications in both low-noise and high-power GaAs MESFET amplifiers, as well as monolithic microwave integrated circuits. In May 1981, he joined the Torrance Research Center of Hughes Aircraft Company, where he was responsible for the development of various monolithic low-noise and power amplifiers, as well as monolithic components for receive and T/R modules operating from *S*-band to *Ka*-band. In February 1986, he joined TRW as assistant department manager of the Advanced Technology Department. He is currently responsible for several monolithic circuit development projects.

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Carol S. Liu (M'86) received the B.S. degree in electrical engineering from the University of California at Los Angeles in 1983. She is currently in the Hughes Fellowship program for the M.S. degree in microwave engineering from the California State University, Northridge.

She joined Torrance Research Center at Hughes Aircraft Company as a member of the Technical Staff in the monolithic GaAs IC section. Her responsibilities include the design and development of MMIC amplifiers and receiver components.

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Joel R. Kessler (S'80–M'84) received the B.S.E.E. degree in 1983 and the M.S.E.E. degree in 1984, both from Purdue University, West Lafayette, IN.

From 1984 to 1986, he was a member of the Technical Staff at Hughes Aircraft Co., Torrance Research Center, working on GaAs MMIC processing. He is currently working towards a Ph.D. degree in electrical engineering at the University of Illinois, Urbana.

Mr. Kessler is a member of Tau Beta Pi and Eta Kappa Nu.

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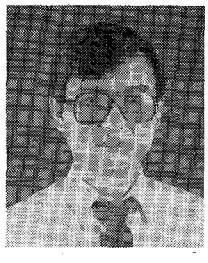

Shing-Kuo Wang (M'76) was born in China on September 25, 1945. He received the B.S. degree in physics from National Taiwan University in 1966 and the M.S. degree in physics and the Ph.D. degree in solid-state physics from Carnegie-Mellon University, Pittsburgh, PA, in 1969 and 1973, respectively.

He joined Hughes Aircraft Company, Torrance Research Center, in 1983, where he is currently Assistant Manager of the Device and Material Technology Department, responsible for the development of GaAs FET devices and MMIC fabrication technology. Prior to joining Hughes, he was a Senior Engineer at the Westinghouse Research Center in Pittsburgh, PA. There he was involved with GaAs material processing, device modeling, and monolithic IC fabrication technology.

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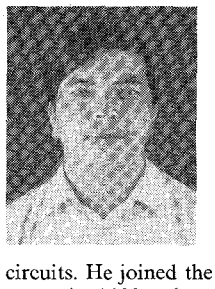

Ching-Der Chang (S'80–M'81) was born in Taiwan, China, on January 22, 1950. He received the B.S. degree from National Cheng-Kung University, Taiwan, in 1972. In 1977, he received the M.S. degree in applied science and in 1981 the Ph.D. degree in electrical engineering, both from the University of California at Davis.

In 1981, he joined the Westinghouse Research and Development Center in Pittsburgh, PA. He has been working on the fabrication and evaluation of GaAs monolithic microwave integrated circuits. He joined the Torrance Research Center, Hughes Aircraft Company, in 1983, where he is currently Head of the Monolithic Circuit Section and is responsible for the development of GaAs monolithic power amplifiers and other MMIC programs such as FET switches, mixers, and receivers.